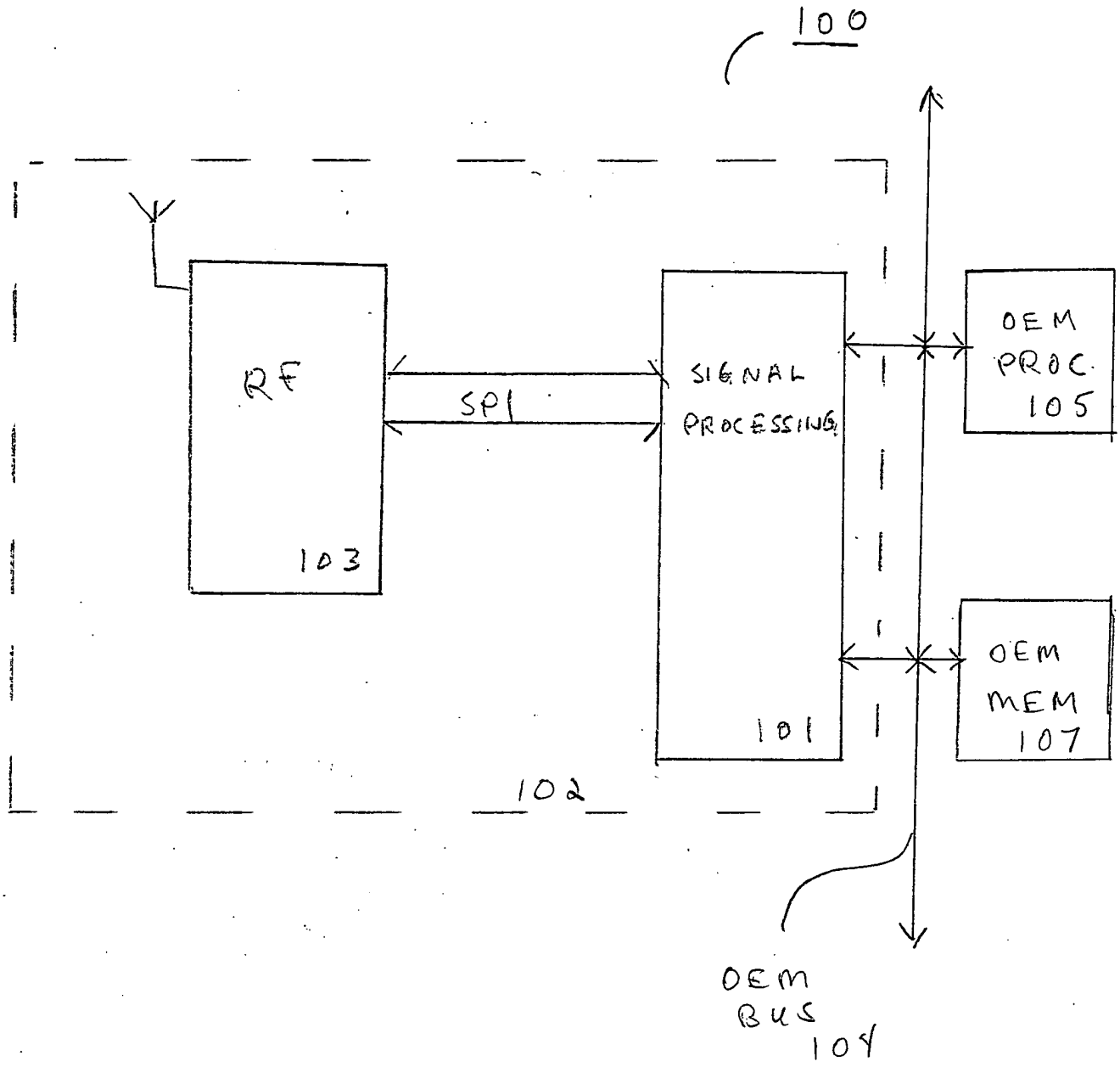

100
RF
103
SPI
SIGNAL
PROCESSING
101
OEM
PROC
105
OEM
MEM
107
102
OEM
BUS
104

FIG. 1

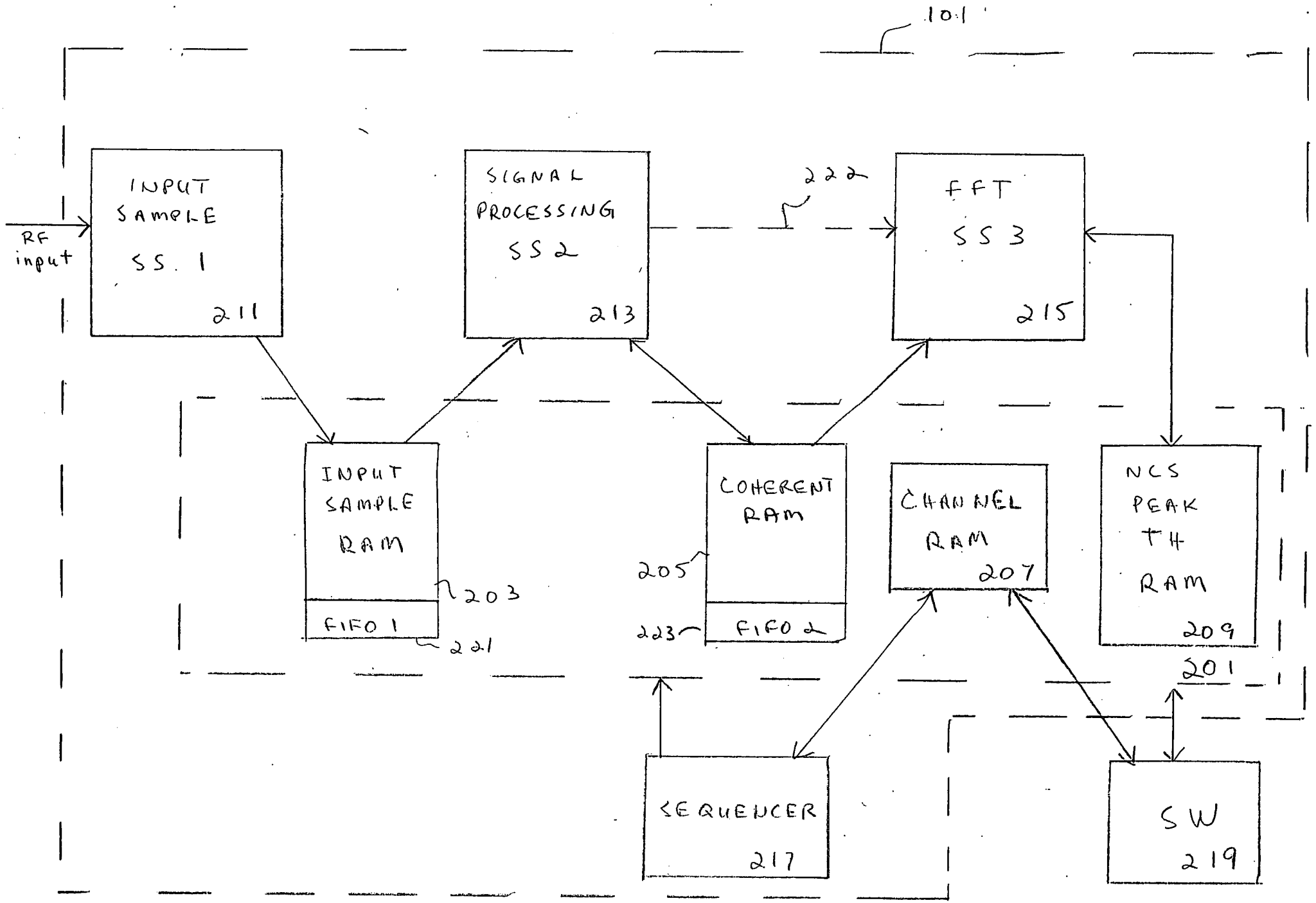

101
RF input
INPUT SAMPLE SS. 1
211
SIGNAL PROCESSING SS 2
213
222
FFT SS 3
215
INPUT SAMPLE RAM
203
FIFO 1
221
COHERENT RAM
205
223
FIFO 2
CHANNEL RAM
207
NCS PEAK TH RAM
209
201
SEQUENCER
217
SW
219

FIG. 2

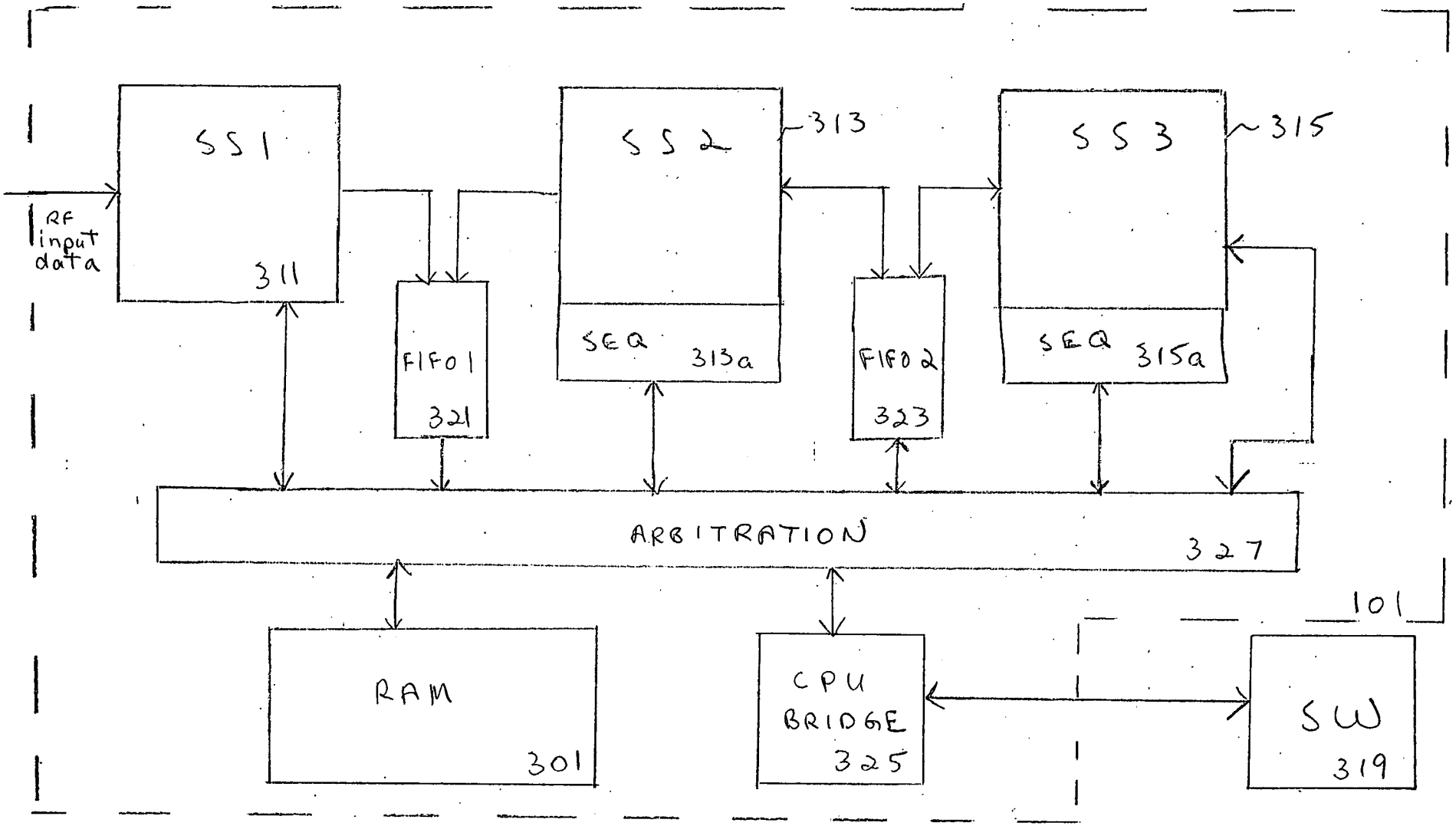

SS1
311
RF input data
FIFO1
321
SS2
313
SEQ
313a
FIFO2
323
SS3
315
SEQ
315a
ARBITRATION
327
101
RAM
301
CPU BRIDGE
325
SW
319

FIG. 3

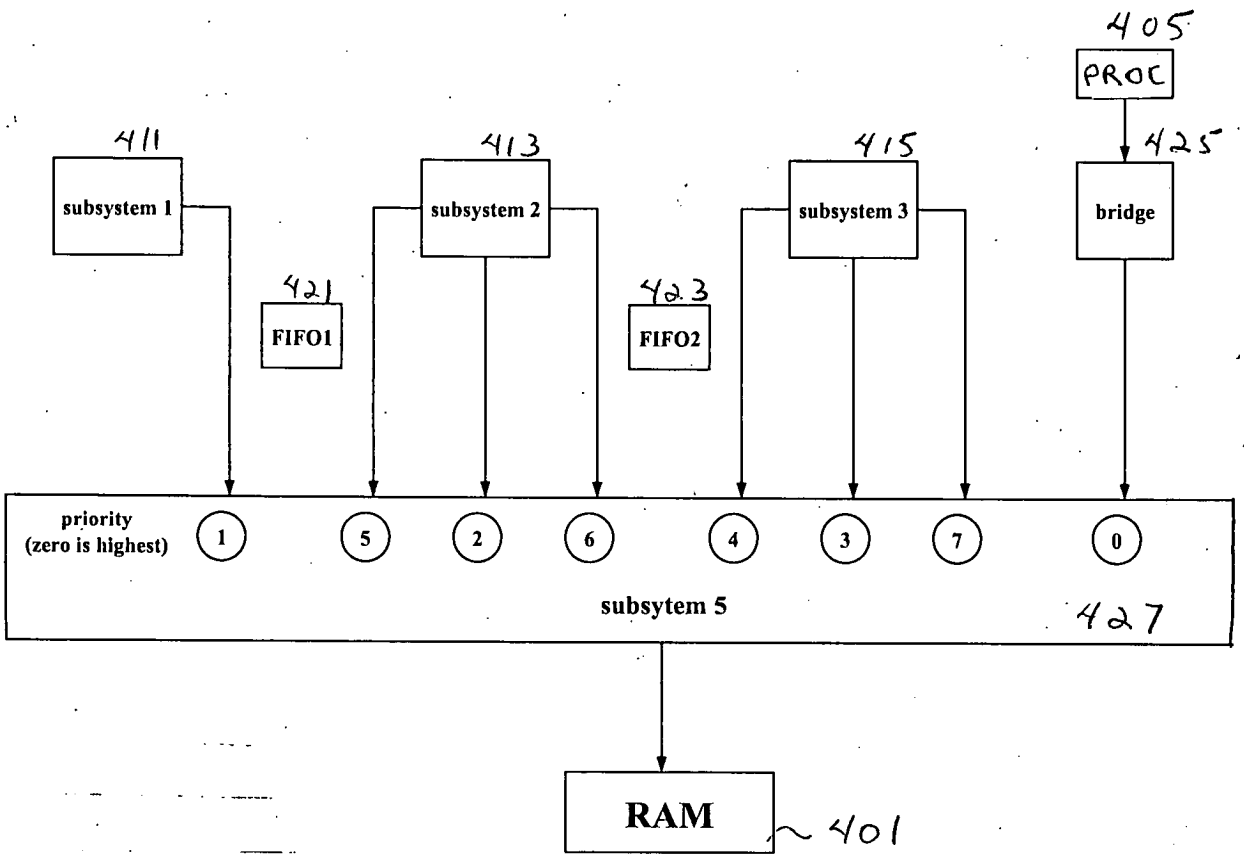

405
PROC
425
411
subsystem 1
413
subsystem 2
415
subsystem 3
bridge
421
FIFO1
423
FIFO2
priority
(zero is highest)
1
5
2
6
4
3
7
0
subsytem 5
427
RAM
401

FIG. 4

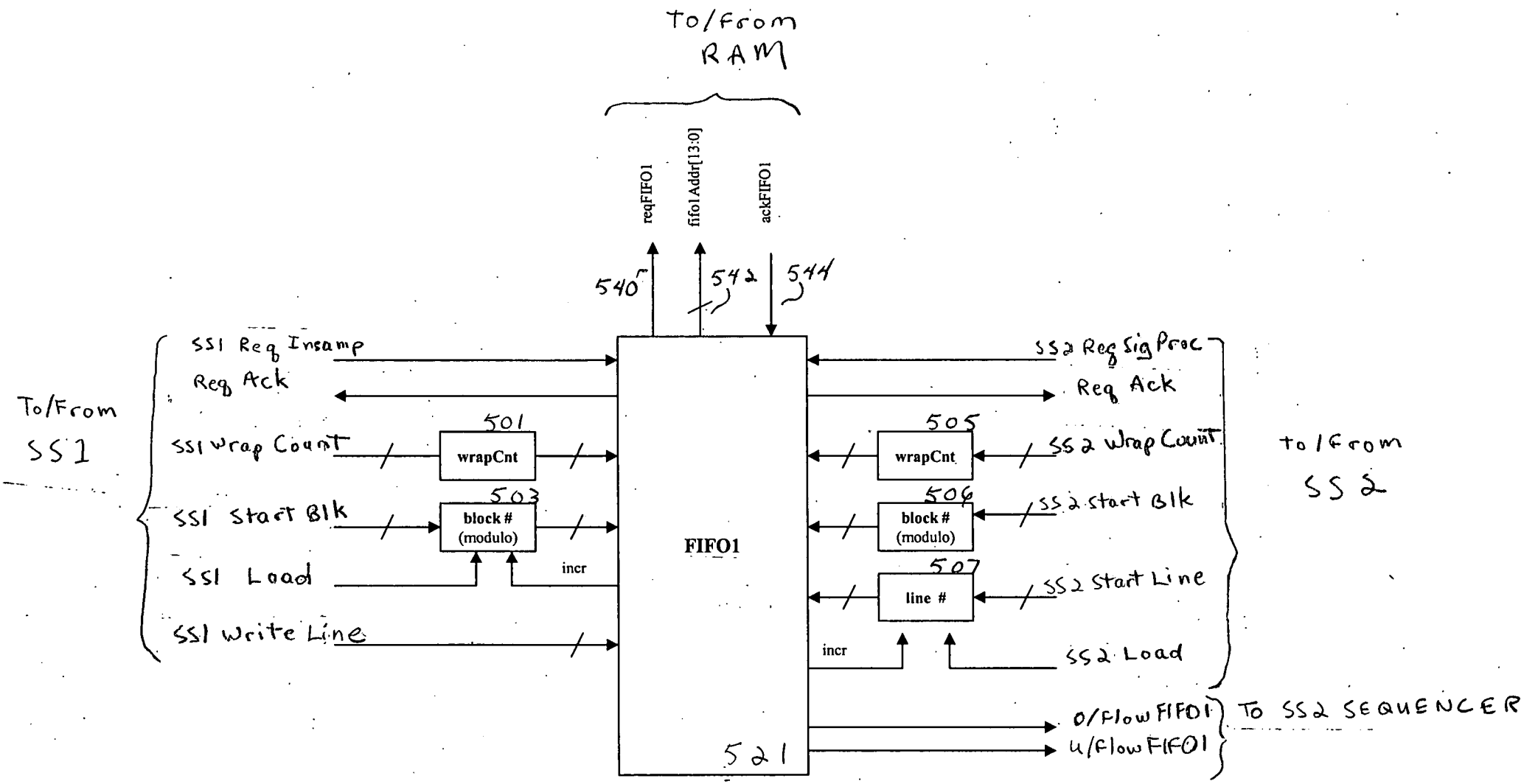

To/From RAM
reqFIFO1
fifo1Addr[13:0]
ackFIFO1
540
542
544
To/From SS1
SS1 Req Insamp
Req Ack
SS1 wrap Count
SS1 start Blk
SS1 Load
SS1 Write Line
501
wrapCnt
503
block # (modulo)
incr
FIFO1
521
SS2 Req SigProc
Req Ack
505
wrapCnt
SS2 Wrap Count
506
block # (modulo)
SS2 start Blk
507
line #
SS2 Start Line
incr
SS2 Load
To/From SS2
O/Flow FIFO1
U/Flow FIFO1
TO SS2 SEQUENCER

FIG. 5

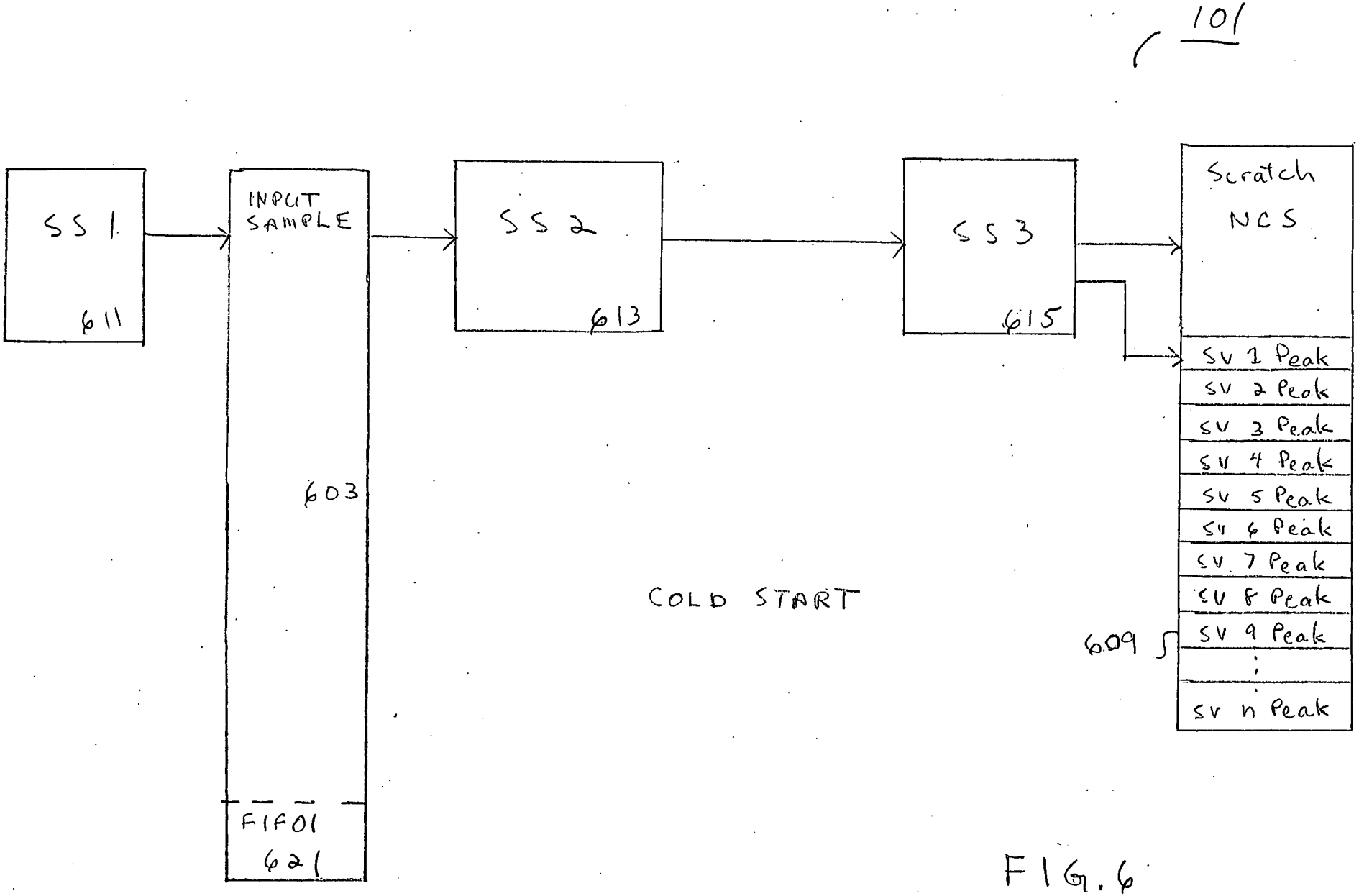
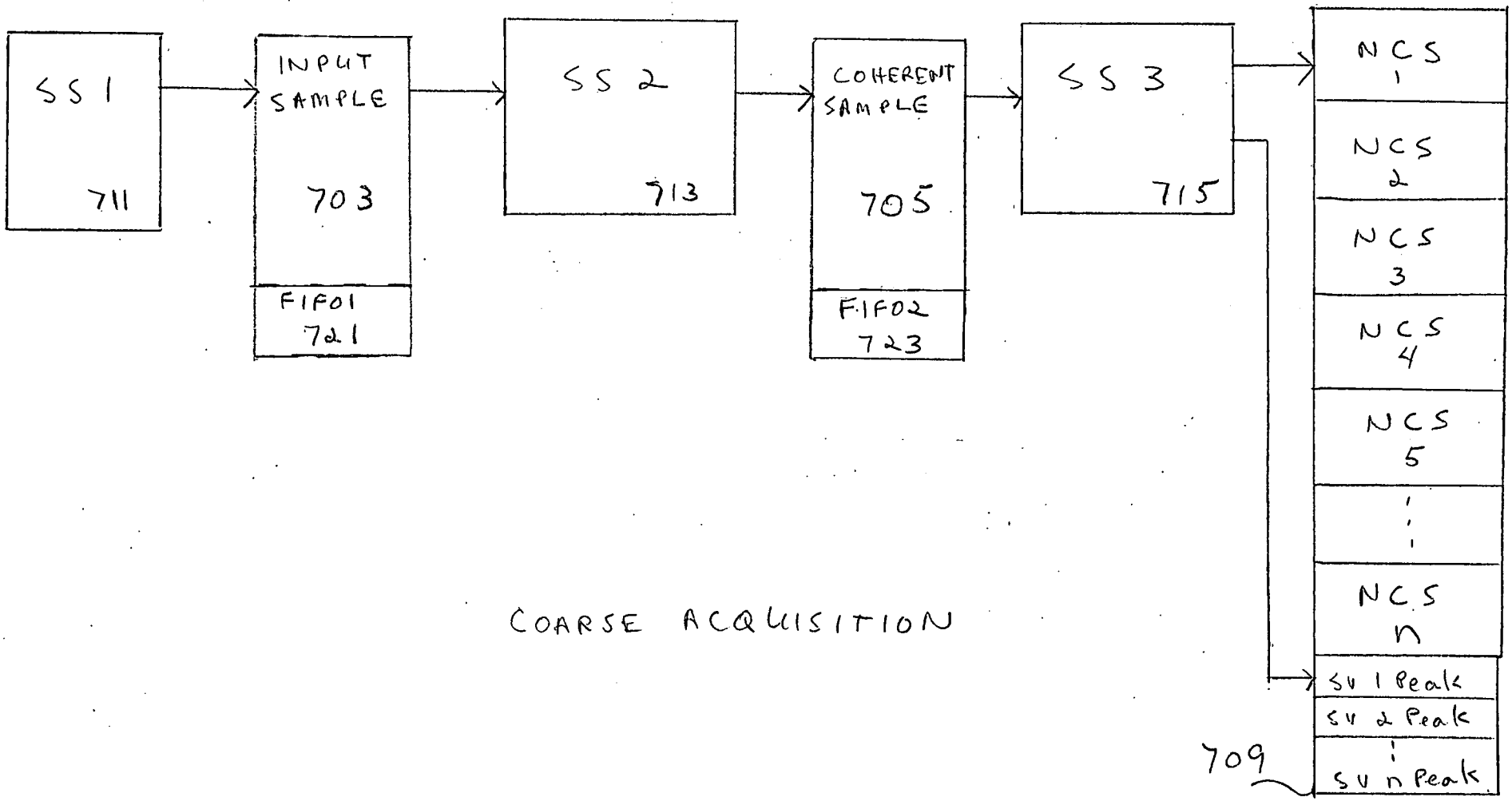
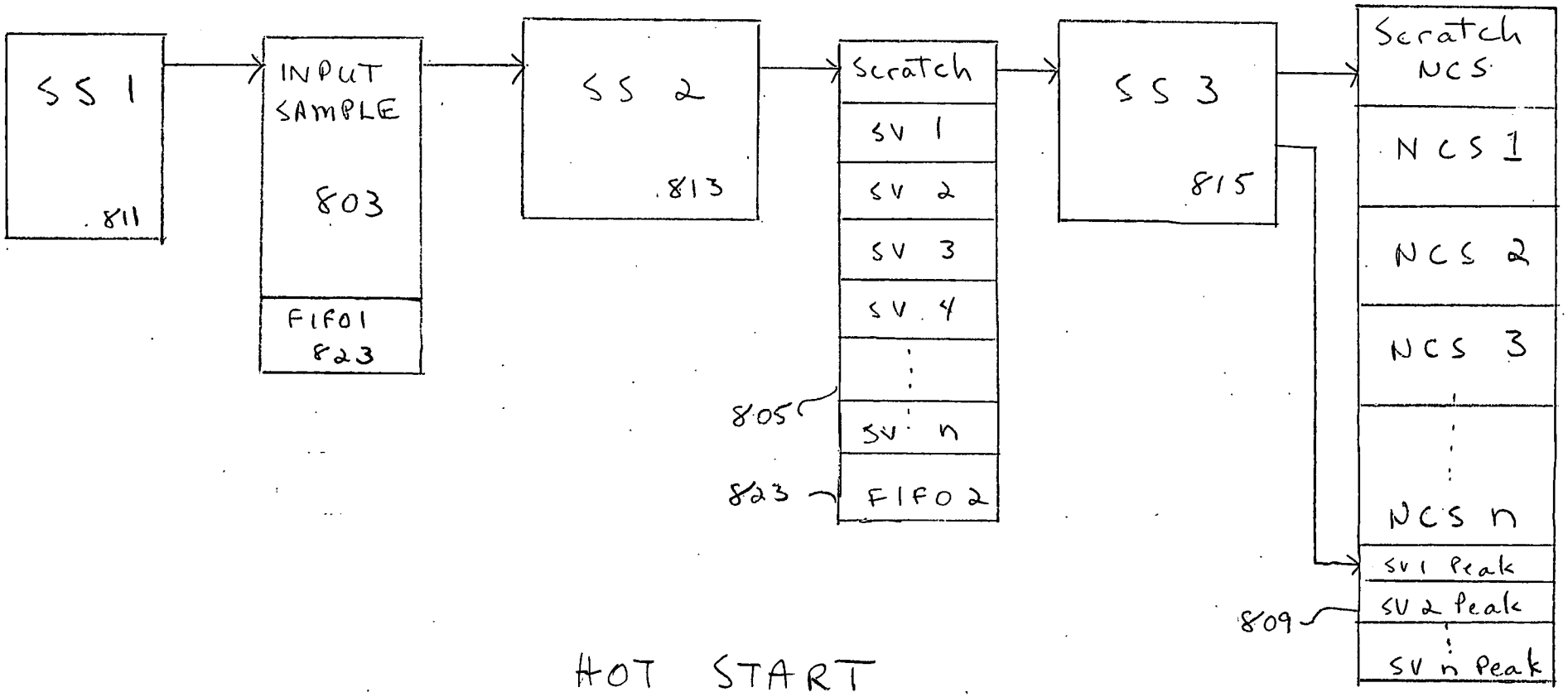

101
SS 1
611
INPUT SAMPLE
603
FIFO1
621
SS 2
613
SS 3
615
Scratch NCS
sv 1 Peak
sv 2 Peak
sv 3 Peak
sv 4 Peak
sv 5 Peak
sv 6 Peak
sv 7 Peak
sv 8 Peak
sv 9 Peak
sv n Peak
609
COLD START

FIG. 6



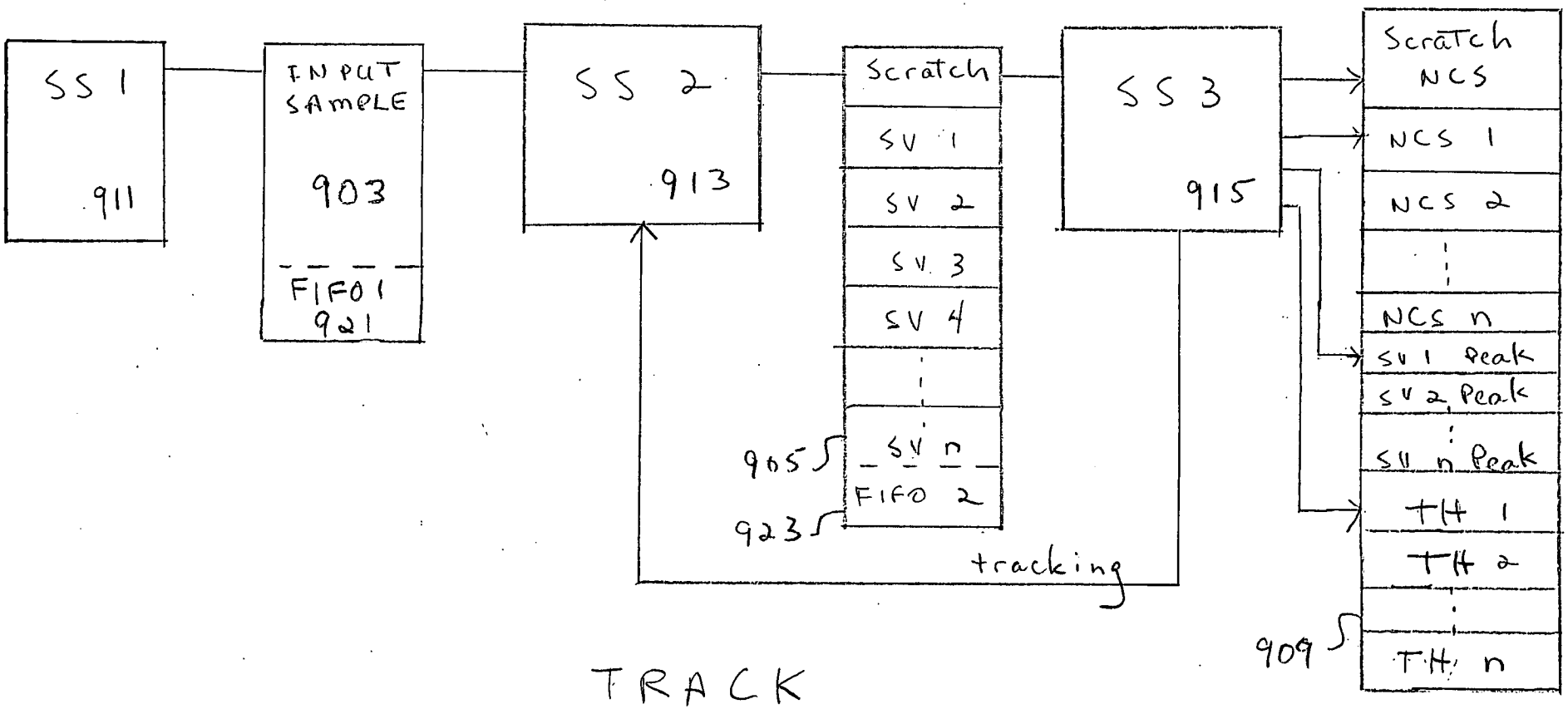
COARSE ACQUISITION

FIG. 7



HOT START

FIG. 8


SS 1
911
INPUT SAMPLE
903
FIFO 1
921
SS 2
913
Scratch
SV 1
SV 2
SV 3
SV 4
SV n
FIFO 2
905
923
SS 3
915
tracking
Scratch NCS
NCS 1
NCS 2
NCS n
sv 1 Peak
sv 2 Peak
sv n Peak
TH 1
TH 2
TH n
909

TRACK

FIG. 9

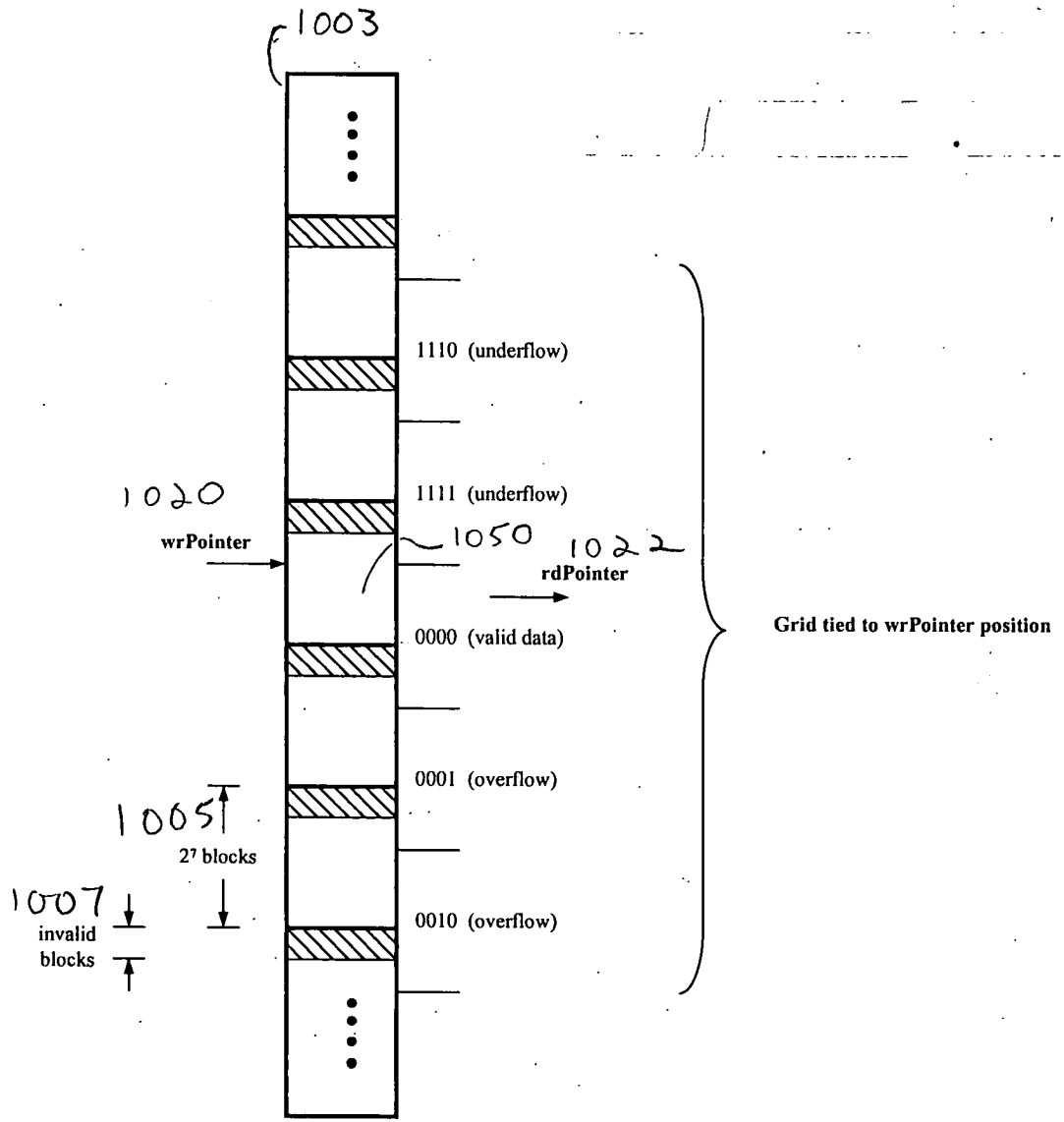

1003
1110 (underflow)
1020
1111 (underflow)
wrPointer
1050
1022
rdPointer
0000 (valid data)
Grid tied to wrPointer position
0001 (overflow)
1005
2⁷ blocks
1007
invalid blocks
0010 (overflow)

FIG. 10

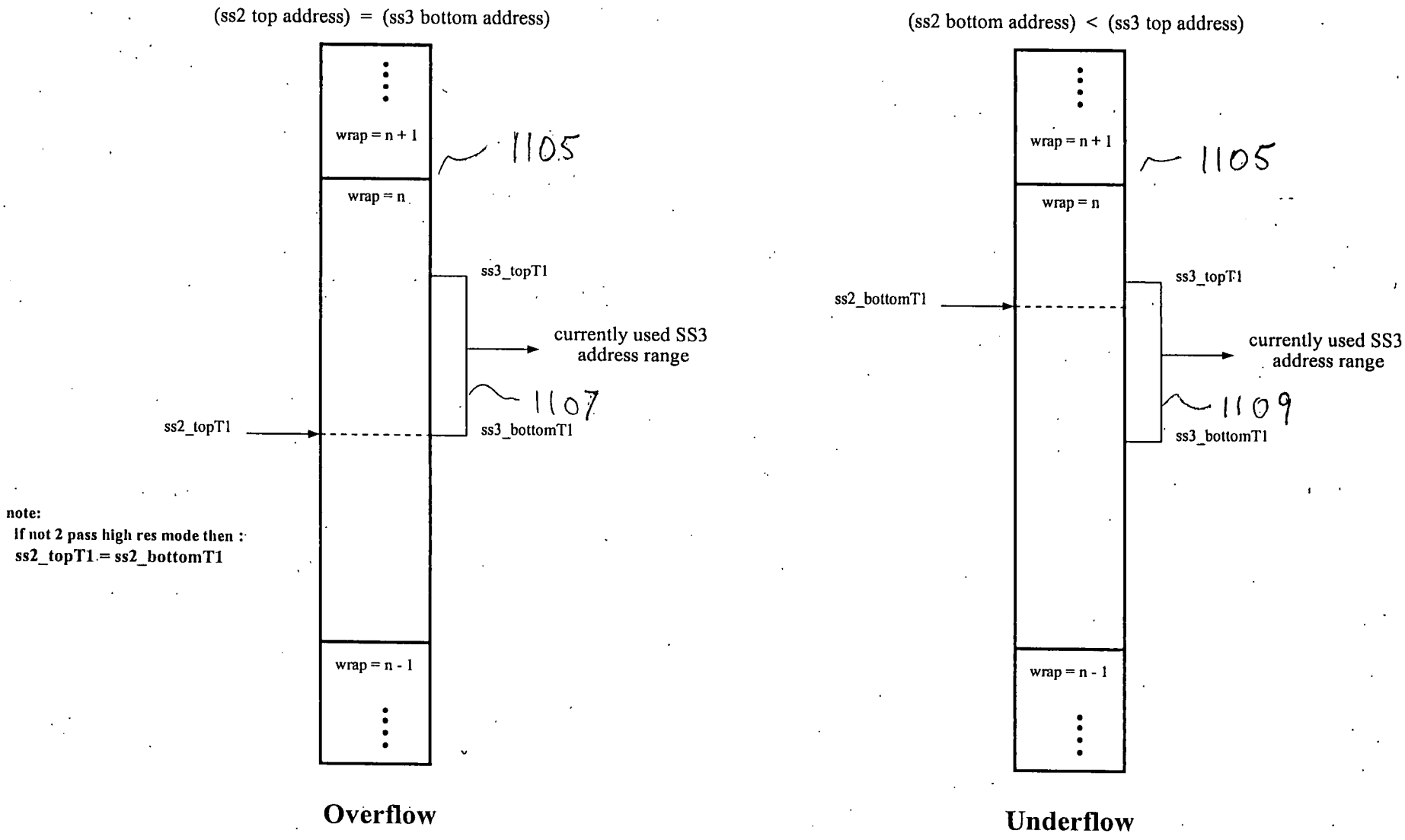

(ss2 top address) = (ss3 bottom address)
wrap = n + 1
1105
wrap = n
ss3_topT1
currently used SS3 address range
1107
ss2_topT1
ss3_bottomT1
note:
if not 2 pass high res mode then :
ss2_topT1 = ss2_bottomT1
wrap = n - 1
Overflow
(ss2 bottom address) < (ss3 top address)
wrap = n + 1
1105
wrap = n
ss2_bottomT1
ss3_topT1
currently used SS3 address range
1109
ss3_bottomT1
wrap = n - 1
Underflow

FIG. 11

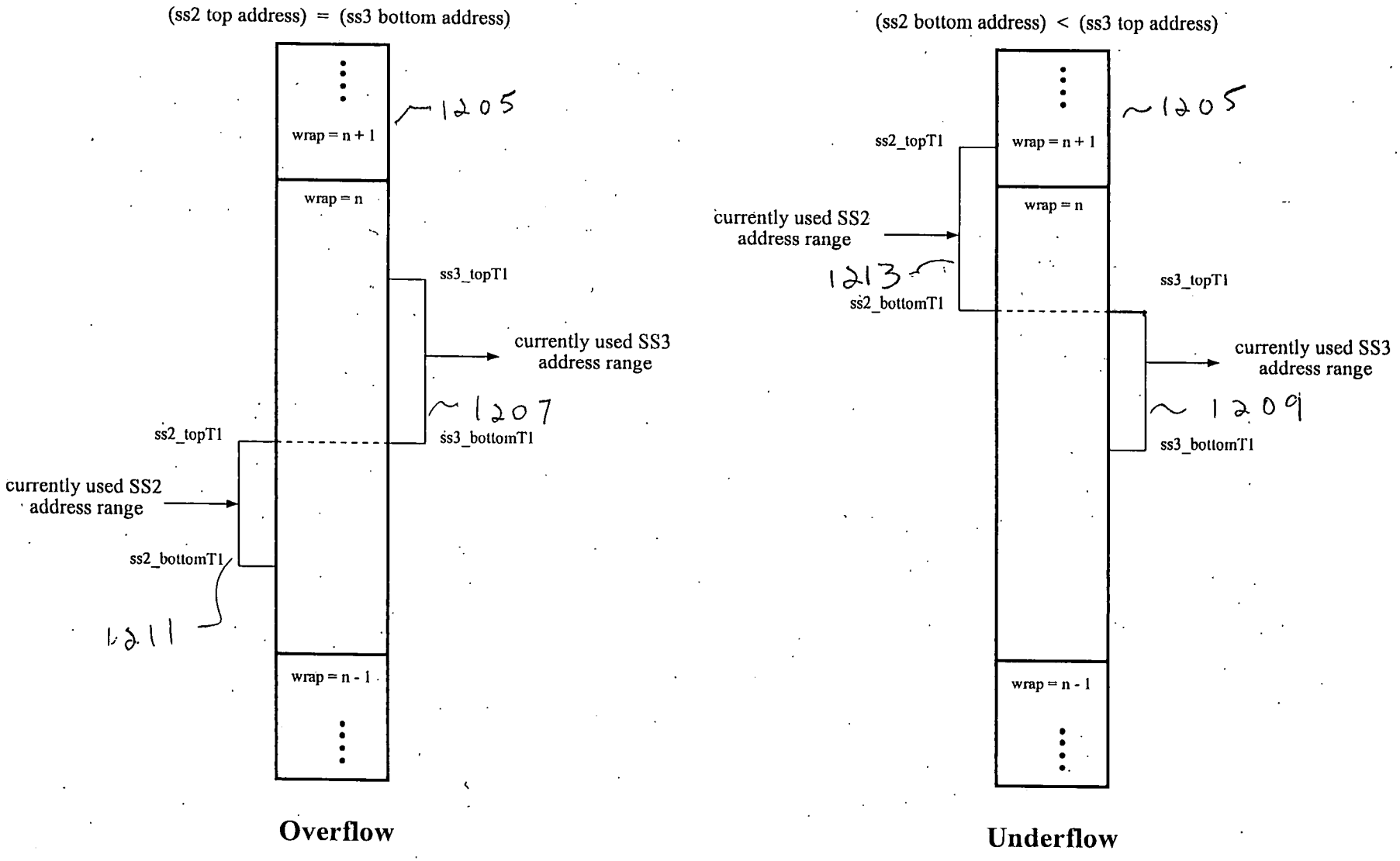

(ss2 top address) = (ss3 bottom address)
wrap = n + 1
1205
wrap = n
ss3_topT1
currently used SS3
address range
1207
ss3_bottomT1
ss2_topT1
currently used SS2
address range
ss2_bottomT1
1211
wrap = n - 1
Overflow
(ss2 bottom address) < (ss3 top address)
1205
ss2_topT1
wrap = n + 1
wrap = n
currently used SS2
address range
1213
ss2_bottomT1
ss3_topT1
currently used SS3
address range
1209
ss3_bottomT1
wrap = n - 1
Underflow

FIG. 12

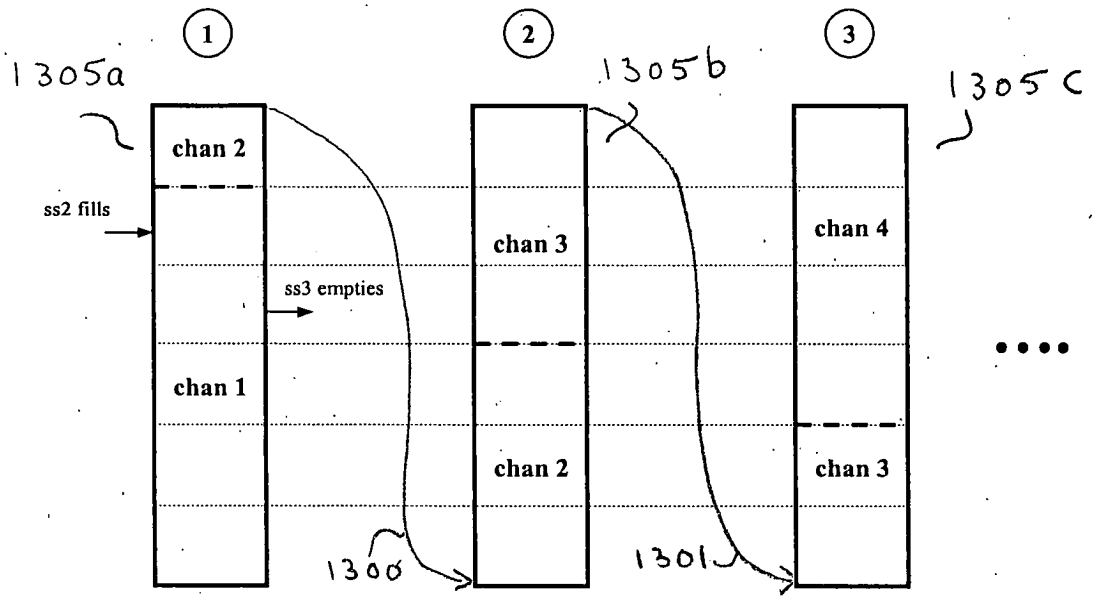

1
2
3
1305a
1305b
1305c
chan 2
ss2 fills
ss3 empties
chan 1
chan 3
chan 2
chan 4
chan 3
1300
1301

FIG. 13

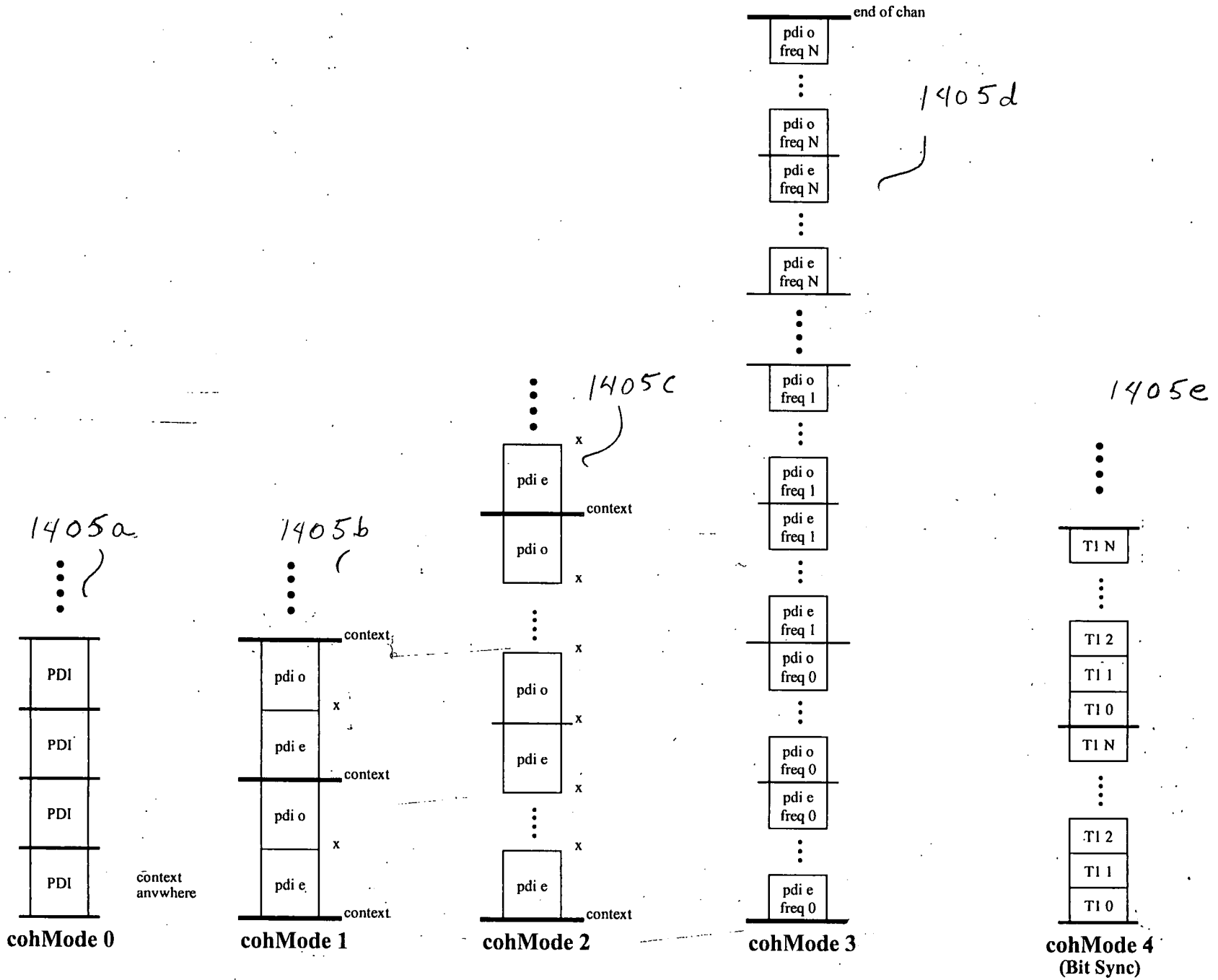

1405a
1405b
1405c
1405d
1405e
PDI
PDI
PDI
PDI
context anywhere
cohMode 0
context
pdi o
x
pdi e
context
pdi o
x
pdi e
context
cohMode 1
x
pdi e
context
pdi o
x
pdi o
x
pdi e
x
pdi e
context
cohMode 2
end of chan
pdi o freq N
pdi o freq N
pdi e freq N
pdi e freq N
pdi o freq 1
pdi o freq 1
pdi e freq 1
pdi e freq 1
pdi o freq 0
pdi o freq 0
pdi e freq 0
pdi e freq 0
cohMode 3
T1 N
T1 2
T1 1
T1 0
T1 N
T1 2
T1 1
T1 0
cohMode 4
(Bit Sync)

FIG. 14

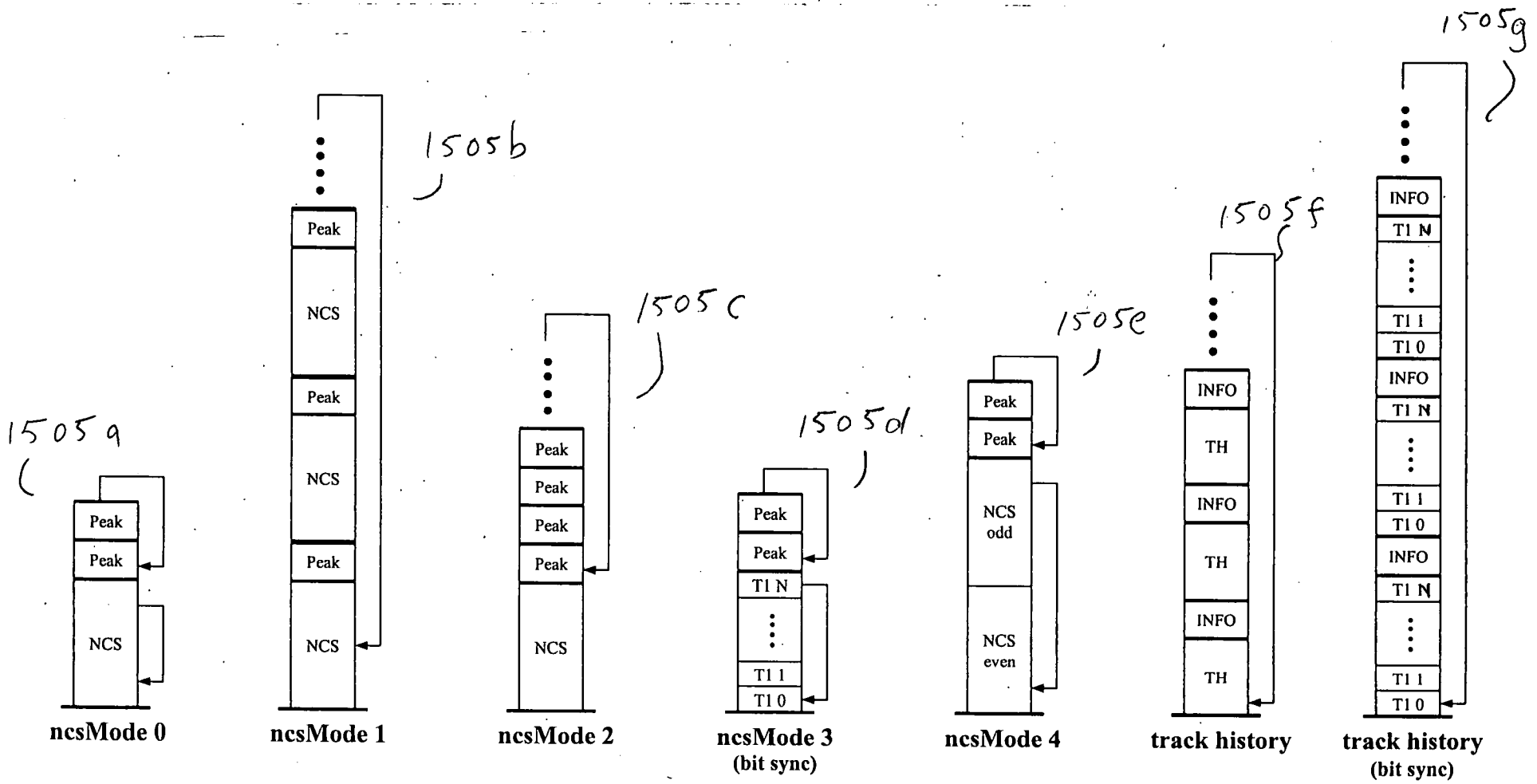

1505a
Peak
Peak
NCS
ncsMode 0
1505b
Peak
NCS
Peak
NCS
Peak
NCS
ncsMode 1
1505c
Peak
Peak
Peak
Peak
NCS
ncsMode 2
1505d
Peak
Peak
T1 N
T1 1
T1 0
ncsMode 3
(bit sync)
1505e
Peak
Peak
NCS
odd
NCS
even
ncsMode 4
1505f
INFO
TH
INFO
TH
INFO
TH
track history
1505g
INFO
T1 N
T1 1
T1 0
INFO
T1 N
T1 1
T1 0
INFO
T1 N
T1 1
T1 0
track history
(bit sync)

FIG. 15

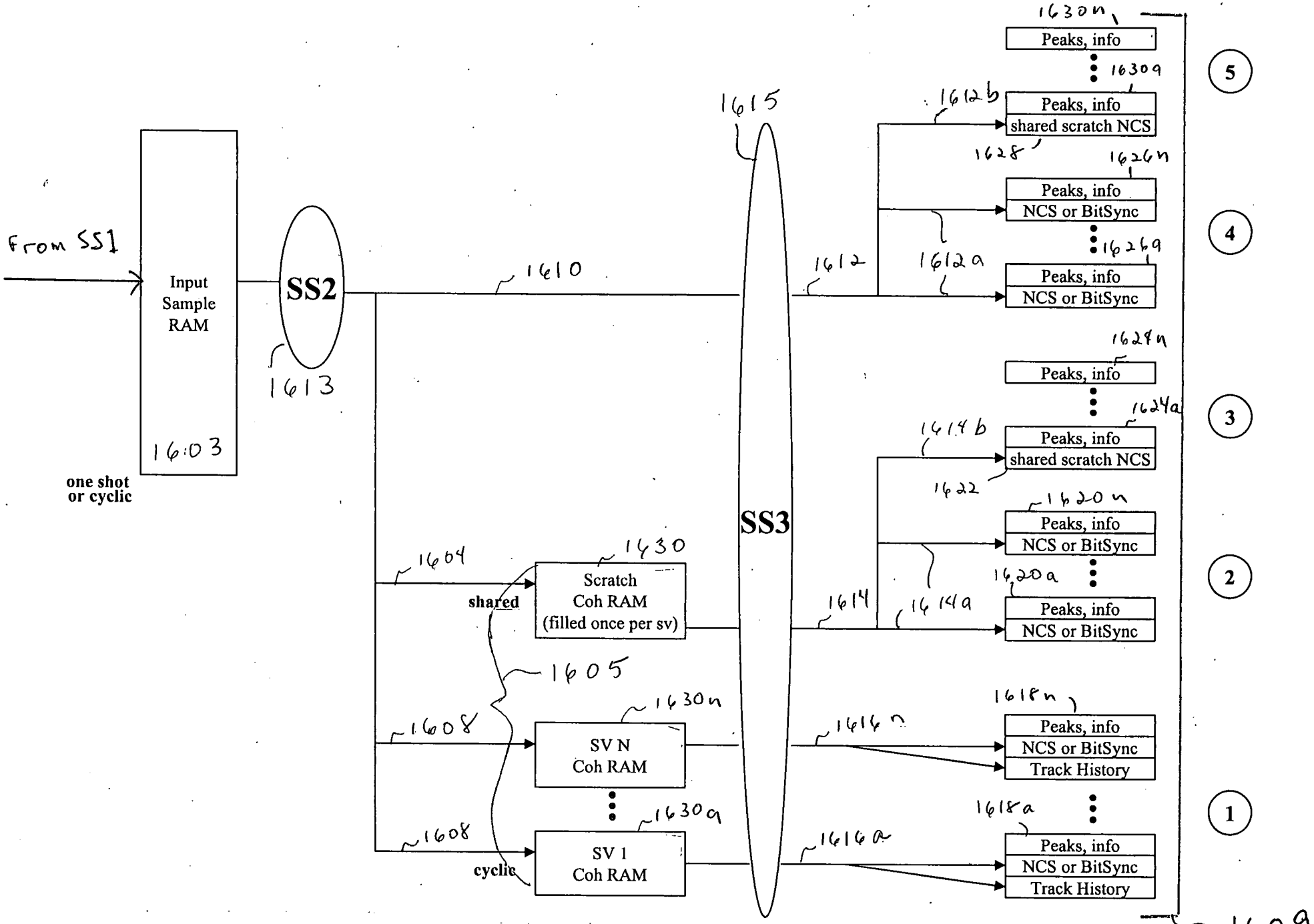

From SS1
Input Sample RAM
1603
one shot or cyclic
SS2
1613
1610
SS3
1615
1612
1612a
1612b
1628
1626n
1626a
1628n
1624a
1614b
1622
1620n
1620a
1614
1614a
1616n
1616a
1618n
1618a
Peaks, info
NCS or BitSync
shared scratch NCS
Track History
1604
shared
1630
Scratch Coh RAM (filled once per sv)
1605
1608
1630n
SV N Coh RAM
1630a
SV 1 Coh RAM
cyclic
5
4
3
2
1
1609

FIG. 16